**REPLY UNDER 37 CFR 1.116**
**EXPEDITED PROCEDURE - 2812**


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## FACSIMILE COVER SHEET

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| To: Examiner Jennifer M. Kennedy | Total Pages Sent: 5 |
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant: | Yeo, *et al.* | Docket No.: | TSM03-0553 |
| Serial No: | 10/667,871 | Art Unit: | 2812 |
| Date Filed: | September 22, 2003 | | |
| Title: | Resistor with Reduced Leakage | | |

## CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 571-273-8300 on the date shown above:

- Certification of Facsimile Transmission (1 page)
- Response After Final Rejection (4 pages)

Respectfully submitted,

AnneMarie James
Legal Assistant

**Confirmation Respectfully Requested**

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE AFTER FINAL REJECTION

Dear Sir:

In response to the Office Action mailed August 24, 2005, Applicant provides the following remarks and requests allowance of all pending claims.

Claims 60-89 are pending in the present application, with claims 64 and 76-79 having been withdrawn as being directed to an unelected species. No claims are amended here. Claim 60 is generic and, therefore, allowance of claim 60 over the prior art will lead to allowance of claims 61-89.

Each of the pending claims has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nowak et al. (U.S. Patent No. 6,100,153, hereinafter "Nowak") in view of Yu et al. (U.S. Patent No. 6,784,101, hereinafter "Yu"), either in combination or in combination with other references. Applicant respectfully traverses this rejection.

Applicant respectfully submits that the explicit teachings of Nowak and Yu teach away from the combination suggested in the Office Action. The following facts are admitted by both Applicant and the Office Action:

- Claim 60 recites the formation of a resistor with a dielectric layer comprising a material with a relative permittivity greater than 8 between a resistor body and a conductive top electrode.
- Neither Nowak nor Yu teach a structure that includes all three of these elements.
- Nowak's prior art Figure 1, and related discussion in lines 45-67 of column 1, illustrates a resistor with a dielectric layer between a resistor body and a conductive top electrode.
- Nowak does not disclose that the dielectric layer comprises a material with a permittivity greater than about 8.
- Yu teaches a transistor that includes a dielectric layer comprising a material with a relative permittivity greater than 8 between a channel and a gate electrode.

The issue in the application is whether or not it would have been obvious to one of ordinary skill in the art at the time of invention to modify the Nowak structure to include a high-k dielectric as taught by Yu. The references themselves make it clear that such a combination would not be obvious. In fact, Nowak explicitly teaches away from such a combination.

Nowak teaches that there were two known types of buried resistors at the time of his invention. One of these is illustrated in Figure 1 and relied upon in the Office Action. Nowak explicitly teaches that this Figure 1 structure is undesirable since the polysilicon is highly doped, i.e., the top electrode comprises a conductive material, and thus "the parasitic capacitance of the buried resistor to polysilicon layer is high." Col. 1, lines 48-52. Nowak repeatedly teaches that low capacitance between the resistor body and the top electrode is desired. Col. 1, lines 31-33 (stating low gate capacitance is a desirable characteristic); col. 2, lines 19-22 (touting the invention because

it "reduces the parasitic diffusion-to-polysilicon capacitance"); col. 3, lines 8-15 (listing the advantages of the new design including "low parasitic diffusion to polysilicon gate capacitance").

Given the very clear teachings of Nowak, Applicant respectfully submits that it would not be obvious to modify the structure disclosed therein in a manner that increases the capacitance between the buried resistor and the top electrode. However, a dielectric layer comprising a material with a relative permittivity greater than 8 included between the buried resistor and the top electrode would increase the capacitance. In other words, Nowak teaches away from making this modification.

To support a rationale to combine the two references, the Office Action states that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate of Nowak et al. by the method of Yu et al. to form a high k dielectric layer because it allows for greater device speed with less gate-to-channel leakage current such that there is overall improved device performance (see Yu et al. column 2, lines 4-30)." A review of this section makes it clear that what may be improved transistor device performance for Yu is an undesirable characteristic for the resistor device of Nowak.

In particular, in the section cited in the Office Action, Yu states that "[t]he increased capacitance k (or permittivity $\epsilon$) of the gate dielectric material advantageously results in an increase in the gate-to-channel capacitance, which in turn results in improved device performance." Col. 2, lines 19-22. This is precisely what Nowak teaches to avoid. In other words, Nowak explicitly teaches away from that which is taught by Yu and thus combination of the references is improper. Since references cannot be combined, the claims must be allowed.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at the address below.

No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

October 10, 2005
Date

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